

Abstract

Test switching circuit for a high speed data interface
5 (1) of an integrated circuit comprising switching trans-
sistors (T1 - T6) which switch in a test mode a termina-
tion resistor output stage (15) of a data transmission
signal path (17) to a termination resistor input stage
(18) of a data reception signal path (25) to form an in-
10 ternal feedback test loop within said integrated cir-
cuit.

(Figure 6)